Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		("(microadjstructuremicrostructure)with(gripermanipulator)").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/27 12:43
L1	2166	(stack$3 near3 gate) with (sidewall side near3 wall spacer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:47
L2	2188	(stack$3 near3 gate) with (sidewall side near3 wall spacer linning liner)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:50
L3	1606	2 and (etch$3 with (sidewall side near3 wall spacer linning liner))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:52
L4	1364	2 and silicide	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:52
L5	511	4 and (bitline bit adj line)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:53
L6	441	5 and ((dielectric insulat$3) with (opening trench hole contact via))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:55
L7	319	6 and (etch$3 with (partial$2 wiht expos$3))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:57
L8	319	7 and gate	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:57
L9	317	8 and substrate	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 13:08
L10	195	9 and (gate with cap$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 13:09
L11	1	"6066541".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
L12	1	"6043529".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
L13	1	"5989952".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20

L14	1	"5972747".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
L15	1	"5929526".PN	USPAT; USOCR	OR	ON	2004/12/27 16:20
L16	1	"6136651".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:31
L17	1	"5998262".PN	USPAT; USOCR	OR	ON	2004/12/27 16:31
S1	71993	(method process$3) with (side adj wall sidewall spacer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/06/06 10:43
S2	10472	((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S3	8483	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and ((etch$3) with (side adj wall sidewall spacer))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S4	3612	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:42
S5	1636	((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45

S6	1636	(((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S7	364	((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:50
S8	99	(((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)) and (acid with etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:51

S9	10135	(method process$3) with ((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:41
S10	28954	((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S11	22184	(((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S12	13851	((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S13	4977	(((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:46
S14	4977	(((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48

S15	2079	(((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)) and (wet near5 etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48